Design of ring VCO based PLL using 0.25 µm CMOS technology

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Abstract—A low power ring VCO based PLL using injection locking is realized by adopting 0.25µm CMOS technology at 2.5V. We have achieved a shift in the bias level by using pMOS active resistive load. The PLL output frequency is 104.4 MHz, at 5 MHz reference frequency by using injection locking based VCO and active resistive load managed to achieve low power dissipation of 4.98mW at 2.5 V.

Index Terms- Phase Locked Loop, Injection Locking, Ring VCO, Shift Bias Level.

I. INTRODUCTION
PLL is very important building block used in communication, computers and other digital systems. Many digital devices such as Mobile phone, Notebooks operates at very high frequencies for which PLL are used for frequency synthesis, all these devices works on batteries so it becomes very important to design systems which consumes less power. The objective of this dissertation is to design a low power CMOS PLL at 2.5 V using 0.25 µm. In this paper we are designing a VCO using the MOS capacitance and active load resistance which are scalable, consumes less power and occupies less area. Also we are using Injection locking VCO to reduce the phase noise. This paper is organized as follows. Section 2 describes the design of differential injection locked ring VCO and all the necessary building blocks. Section 3 contains the comparison of the work done in this paper. The results are discussed in Section 4 along with the conclusion.

We have used injection locking as there are no stability issues and it also increases the loop bandwidth. The output phase noise tracks injection signal phase noise over wide bandwidth and it is very easy to implement. Injection locking can be used at very high frequencies.

II. DESIGN OF THE DIFFERENTIAL INJECTION-LOCKED RING-VCO
Usually tuning exhibits nonlinearity i.e. $K_{VCO}$ is not constant. Such nonlinearity degrades the settling behavior of PLLs and leads to high sensitivity for some frequency region. To avoid this we need to minimize the variation of $K_{VCO}$ across the whole tuning range. The linearity of the frequency tuning of a VCO is easily seen from its functional dependence of $K_{VCO}$ on the control voltage. The closed loop transfer function of a PLL, $H(s)$ is proportional to $K_{VCO}$. The loop bandwidth is given as:

$$\omega_n = \frac{K_{VCO} I_p}{2\pi N C_f}$$

where $I_p$ is the charge pump current, $N$ is the division ratio of the feedback loop, and $C_f$ is the filter capacitance. So we can see that the loop bandwidth can be changed by varying the $K_{VCO}$\[11\]
Control voltage for VCO is generated by charge pump which passes through the RC filter the transient response of control voltage to VCO is shown above. This response shows that VCO control voltage varies linearly with time.

PFD compares the phase of two input signals one is the clock frequency or reference signal and other is the feedback signal from VCO to frequency divider and to PFD. PFD output is fed to the charge pump circuit. It has two inputs A and B which is applied to the clock terminal of the D flip flop.
Charge pump circuits are capable of high efficiencies, (90–95%) while being electrically simple circuits.

A divide by two circuit commonly called DTC is widely used to produce quadrature outputs.

Fig. 11. Simulation setup of PLL with reference frequency of 5 MHz [1]

Fig. 12. (a) Output response of PLL 104.4 MHz (b) Control voltage for VCO (c) Output response of
frequency divider (d) Reference input signal of 5 MHz

The transient response of the PLL is shown in the figure 6.4 which involves reference signal, VCO output frequency, VCO control voltage, and f/2 output signal which is fed to the PFD.

Fig. 13. Magnified transient response of PLL tested at 4 MHz input reference frequency

In this test setup PLL consumes 4.98 mW at 2.5 V power supply. Its transient power consumption curve is shown below

Fig. 13. Transient power consumption curve of PLL (4.98 mW) at 2.5 V power supply

III. PERFORMANCE SUMMARY OF PLL

TABLE 1

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.25 µm CMOS process</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>2.5 V</td>
</tr>
<tr>
<td>PLL output frequency</td>
<td>104.4 MHz at 5 MHz reference input frequency</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>4.98 mW</td>
</tr>
</tbody>
</table>

IV. CONCLUSION

The design proposed in this dissertation is tested at 5 MHz reference signal but this design can support wide range of reference signal. The purpose of this dissertation is to demonstrate the design at 2.5 V at 0.25 µm CMOS technology. There are various electronic communication systems which operate at such voltage level. This PLL can be used at the radio receiver and super heterodyne demodulators. Design consumes 4.98 mW at 2.5 V power supply which makes it suitable to use in battery operated systems. This design can be implemented at different CMOS technology such as 0.18 µm CMOS technology. Since this design is fully differential, which makes it noise immune.

TABLE 2

<table>
<thead>
<tr>
<th>Tuning range</th>
<th>Phase noise</th>
<th>Power (mW)</th>
<th>CMOS (in nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>5 MHz</td>
<td>4.98</td>
<td>250</td>
</tr>
</tbody>
</table>

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