Performance Analysis of CMOS NOR and NAND Gate using Sleepy Stack Power Dissipation

Mahima Yadav[1], Dr. Laxmi Narayan Gahalod[2], Dr. Soni Changlani[3]

[1]M. Tech Scholar: Department of ECE, LNCT, Bhopal, Madhya Pradesh, India
[2]Associate professor: Department of ECE, LNCT, Bhopal, Madhya Pradesh, India
[3]Professor and Head: Department of ECE, LNCT, Bhopal, Madhya Pradesh, India

Abstract—**In today's world of consumer electronics there is a requirement of high frequency circuits which is having low power consumption so that it can be used in designing battery driven handheld devices. On the other hand there is a huge requirement of CMOS technology compatible device which can be used as power amplifiers for communication devices like repeaters and routers. NAND and NOR gates were implemented using various technique approaches for digital schematic design such as sleepy keeper, stack approach etc. Power utilization analysis of the various method techniques for NAND and NOR gates were implemented. Finally compared the power utilization analysis for the various techniques of the proposed and existing methods. To Survey the various existing research works that are relevant to the proposed research work such as sleepy stack, dual stack, zigzag, forced stack etc. To analyze the power gating and multi-threshold CMOS circuits, input vector control and data driven clock circuits that are relevant to the proposed research work. To implement and power utilization analysis for both NAND and NOR gates using sleepy keeper approach and comparing with various existing methods.**

Index Terms— **NAND Gate, NOR Gate, Sleepy Keeper, CMOS Circuit**

I. INTRODUCTION

Reducing power dissipation has now become a critical design concern in almost all electronic systems. Reduction in the supply voltage is the most significant method for reducing the power dissipation because of the quadratic relationship between the supply voltage and the dynamic power dissipation [1]. To compensate for the performance loss due to a lower supply voltage, threshold voltage of MOS transistors is also reduced. However, this causes an increase in the leakage current. Among all leakage currents, sub threshold leakage current is the most dominant [2]. This leakage current will become a large component in the total power dissipation with further down scaling in technology. Therefore, today an important research area in achieving low power dissipation is to develop effective circuit techniques to reduce this leakage current that is mainly caused by the reduction in the threshold voltage of MOS transistors and down scaling in technology (Roy et al. 2003). Technology scaling has allowed more functions per unit area, and lower dynamic power dissipation, but has also increased the leakage power dissipation exponentially. An analysis of trends based on the International Technology Roadmap for Semiconductors (ITRS) shows that the leakage power dissipation is beginning to exceed the dynamic power dissipation with the down scaling in technology generation, which is shown in Fig. 1. In the past, circuit design techniques and architectures ignored the effects of leakage power dissipation because it was insignificant in comparison with the dynamic power dissipation. However, in modern technologies, the role of subthreshold leakage power dissipation cannot be ignored and now it has become dominant in the overall power dissipation in deep submicron and Nano-scale technologies [3].

Fig. 2 shows the power dissipation in standard CMOS circuits using long channel MOS transistors without scaling in the supply and threshold voltage. Fig. 1.3 demonstrates the increase in the standby leakage power dissipation in standard CMOS circuits using short channel MOS transistors. This demonstrate that the increase in the standby leakage power with technology scaling due to the use of short channel MOS transistors completely cancels the benefit of reduced dynamic and leakage power in active mode with the reduction in the supply voltage [4].
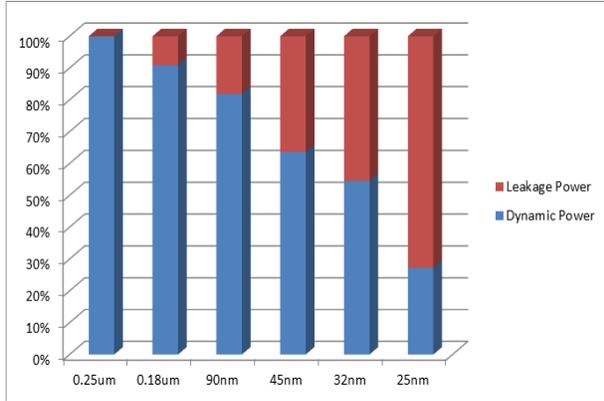
Figure 1.1: Leakage versus dynamic power dissipation trends with technology scaling
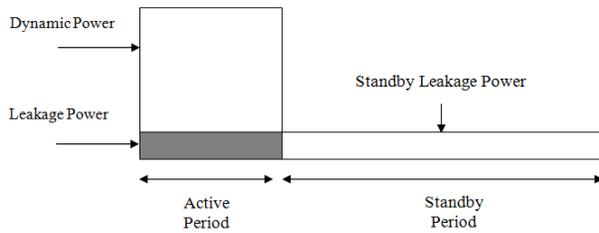
Figure 2: Power dissipation in standard CMOS circuits using long channel MOS transistors without supply and threshold voltage scaling

II. POWER DISSIPATION

Power dissipation in digital logic circuits can be broadly divided into two categories: dynamic power dissipation and static or leakage power dissipation. Dynamic power dissipation is mainly caused by the current flow due to charging and discharging of parasitic capacitances in the logic circuit. Static power dissipation occurs during the static input states of the device. With the down scaling in technology, contribution by static power dissipation increases in the overall power dissipation. In deep submicron CMOS technologies, the role of sub threshold leakage power dissipation becomes dominant among other leakage power components because of down scaling in technology. Under such condition, the static power dissipation is approximately equal to the sub threshold leakage power dissipation and is expressed as

$$P_{Static} \approx P_{Subthreshold}$$

(1)

A general formula for the total power dissipation in a digital logic circuit in deep submicron CMOS technologies can be expressed as

$$P_{total} = P_{dynamic} + P_{static}$$

(2)

$$P_{total} \approx P_{dynamic} + P_{subthreshold}$$

(3)

Where $P_{dynamic}$ is the dynamic power dissipated by the circuit, $P_{subthreshold}$ is the switching component of the power caused by charging/discharging of the circuit output load capacitance C_l, and P_{sc} and P_l reflect the power dissipated due to short- circuit and leakage currents respectively(I_{sc} and I_l). By employing appropriate design techniques both short circuit and leakage current should be reduced to a negligible level leaving the charging and discharging of the node capacitances as the dominant factor of power consumption.

III. PROPSOED METHODOLOGY

The proposed methodology is a sleepy keeper approach to reduce for power consumption. Here, the power consumption is observed by employing the DSCH and MICROWIND tool.
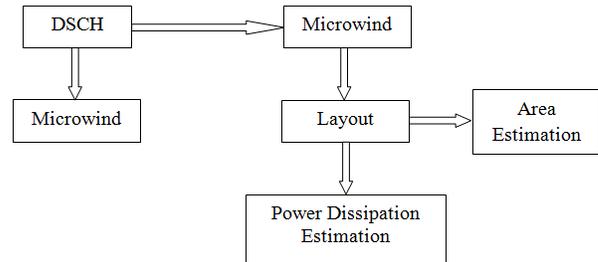
Figure 3: Block diagram

Sleepy Keeper Approach
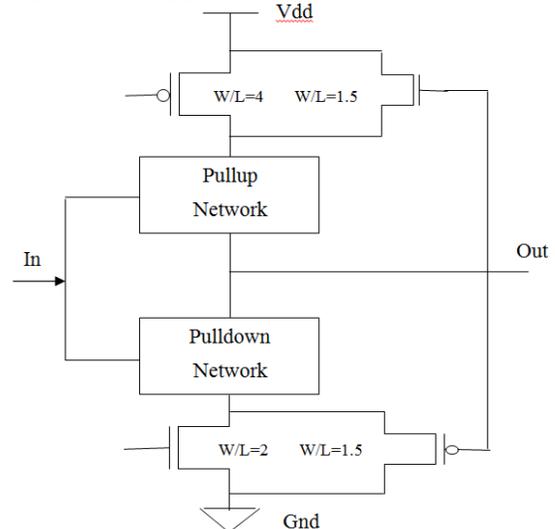
Figure 4: Sleepy keeper approach

The proposed leakage reduction method is known as the sleepy keeper method. The vital concern with conventional CMOS is that the transistors are employed in the most efficient manner. PMOS transistor is applied with VDD supply and NMOS transistor is grounded. However, the PMOS transistors are not effective while dispatching GND. Similarly, the NMOS transistors are not effective at passing VDD. In order to uphold the level '1' during sleep state, the sleepy keeper technique utilizes the output value of '1'. An NMOS transistor is connected to VDD so that the output value is maintained to '1' during sleep state. A supplementary single NMOS transistor connected across the pull-up sleep transistor passes VDD to pull up network. During sleep state, this NMOS transistor is the only source of VDD as the sleep transistor is kept off. As shown in Figure 4, a supplementary single PMOS transistor is placed across the pull-down network. The sleep transistor is the only source of GND to the pull-down network and it is the dual case of the output '1'. Sleepy keeper method consumes the conventional sleep transistors with two extra transistors to keep the state during sleep mode.

IV. SIMULATION RESULTS

Designing Circuits the Figure 5 inferences the digital schematic diagram for basic NAND gate using microwind tool.
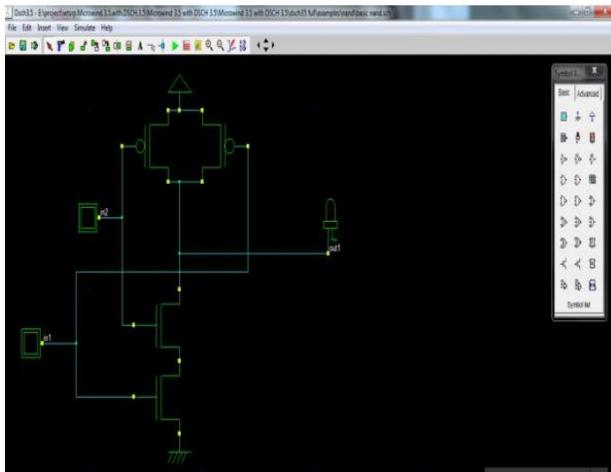
Figure 5: Design of basic NAND gate

The Figure 6 inferences the digital schematic diagram for sleepy keeper approach NAND gate using microwind tool.
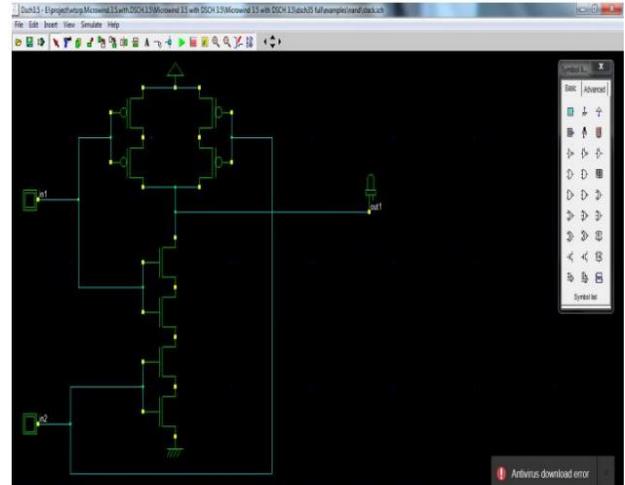
Figure 6: NAND using sleepy keeper approach

The Figure 7 inferences the digital schematic diagram for basic NOR gate using microwind tool.
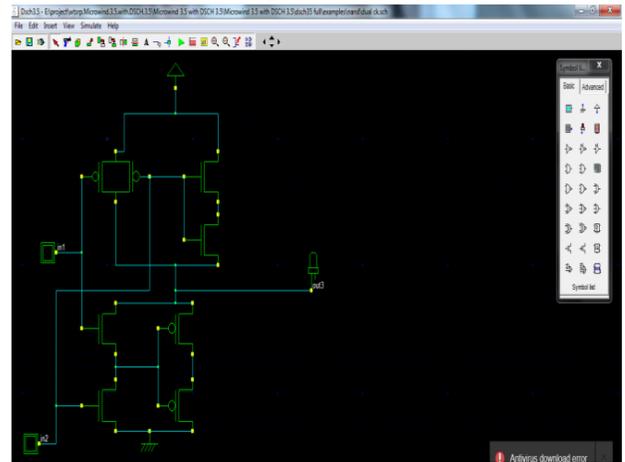
Figure 7: Basic NOR gate

The Figure 8 inferences the digital schematic diagram for stack approach NOR gate using microwind tool.
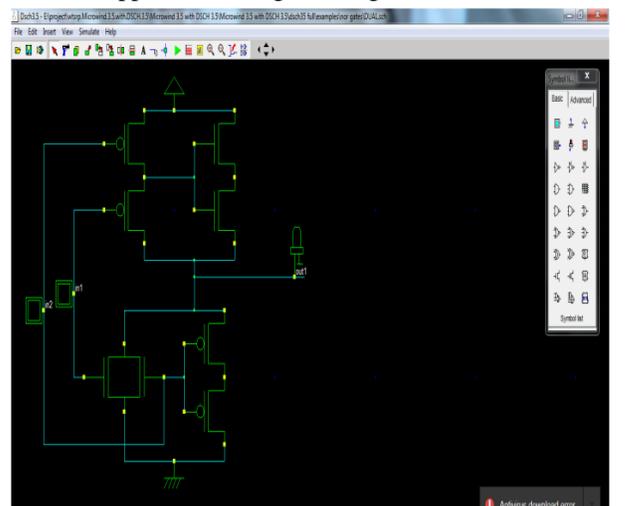
Figure 8: NOR gate using sleepy keeper approach

Table 1 represents the NAND gate using different methods. The basic NAND gate providea power of 3016 nW, Zigzag method provide a power 2328 nW, Stack method provide a power 1183 nW, Dual Stack method provide a power 1033 nW, Sleepy Stack method provide a power 696 nW and Sleepy Keeper method provide a power 595 nW. Fig. 9 shows the graphical representation of the comparison method.

Table 1: Comparison of power utilization of NAND gate using various methods

Method	Power (nW)	
	Previous Sai Srinivas Chandra et al. [1]	Proposed Method
Basic Nand Gate	4036 nW	3016 nW
Zigzag Method	2893 nW	2328 nW
Stack Method	1467 nW	1183 nW
Dual Stack Method	1282 nW	1033 nW
Sleepy Stack Method	899.3 nW	696 nW
Sleepy Keeper Method	829.7 nW	595 nW
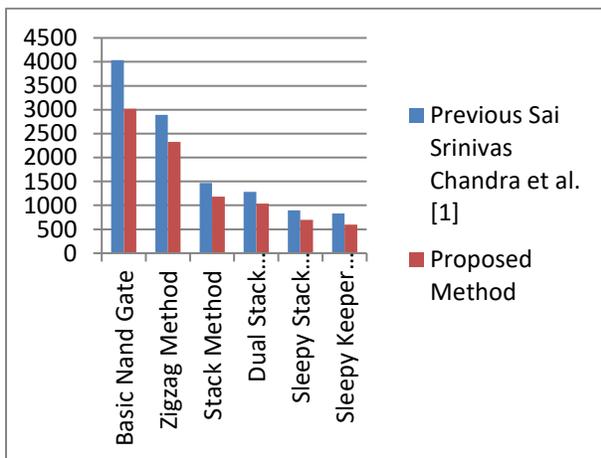
Figure 9: Graphical Represent of NAND Gate

Table 2 represents the NOR gate using different methods. The basic NOR gate providea power of 1437 nW, Zigzag method provide a power 1374 nW, Stack method provide a power 1397 nW, Dual Stack method provide a power 1250 nW, Sleepy Stack method provide a power 706 nW and Sleepy Keeper method provide a power 644 nW. Fig. 10 shows the graphical representation of the comparison method.

Table 2: Comparison of power utilization of NOR gate using various methods

Method	Power (uW)	
	Previous Sai Srinivas Chandra et al. [1]	Proposed Method
Basic NOR Gate	1892 nW	1437 nW
Zigzag Method	1782 nW	1374 nW
Stack Method	1626 nW	1397 nW
Dual Stack Method	1472 nW	1250 nW
Sleepy Stack Method	902.3 nW	706 nW
Sleepy Keeper Method	876.3 nW	644 nW
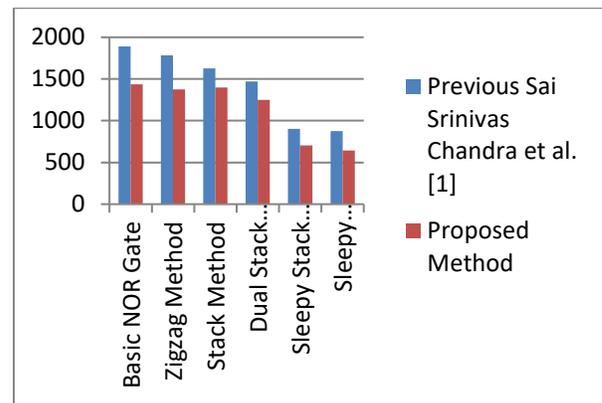
Figure 10: Graphical Represent of NOR Gate

V. CONCLUSION

The main design requirements of integrated circuits (ICs) are based on methods that provide a compromise between Circuit performance and compatibility. The main concern in today's world is hardware confident. The security of computer hardware, especially ICs, is an important aspect of overall security of the computer system. Build a foundry with modern equipment and modern production processes capacity requires a lot of maintenance and involves high construction costs. As a result, fables companies are send their integrated circuits to advanced and well-equipped foundries for production1. As a result, an unscrupulous IC foundry can manufacture ICs and sell them illegally. Furthermore, once the chip is in microchip supply chain, it is also vulnerable to various reverse engineering attacks, for the purpose of extracting drawings or design-specific secret as secret key. Since

attackers know the IC design process, they can quickly reverse engineering the function of an IC/IP. Today, hardware is subject to a number of new types of attacks, including reverse engineering and IP hacking. As a result, IP providers face many challenges to protect IP against piracy, reverse engineering and overproduction.

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