Implementation of systematic cell design methodology for energy efficiency

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***Abstract*- In this paper, a Systematic cell Design Methodology (SCDM) founded on transmission gate within the class of hybrid-CMOS good judgment style is proposed. (SCDM), which is an extension of Cell Design methodology (CDM), plays the fundamental position in designing effective circuits. After that, concerning high flexibility in design targets, SCDM aims to specific ones in the remaining three steps, which are wise selections of basic cells and amend mechanisms, as well as transistor sizing. In the end, the resultant three-input XOR/XNORs enjoy full swing and fairly balanced outputs. We can extend this project for designing of full adder design and it's topologies.**

***Index Terms*- Systematic cell design methodology, three input XOR/XNOR, energy efficiency.**

I. INTRODUCTION

Building low-power VLSI system has emerged as significant performance goal because of the fast technology in mobile communication and computation. As we are aware that the both exclusive-OR (XOR) and exclusive-NOR (XNOR) gates are the main elements of several digital programs and are particularly utilized in very large scale integration (VLSI) methods [1] equivalent to parity checkers, comparators, crypto processors [2] [3], arithmetic and good judgment circuits [4-7], test pattern generators [8], especially in Full adder module as Sum output that's 3-input XOR and so on. In these types of techniques, XOR and XNOR gates constitute part of the critical direction of the procedure, which tremendously affects the worst-case extend and the overall performance of the system.

The exclusive-OR (XOR) and exclusive-NOR (XNOR) gates are the essential parts of several digital systems and are highly used in very large scale integration (VLSI) systems such as parity checkers, comparators, crypto processors, arithmetic and logic circuits, test pattern generators, especially in Full adder module as Sum output that is 3-input XOR and so forth. In most of these systems, XOR and XNOR gates constitute a part of the critical path of the system, which significantly affects the worst-case delay and the overall performance of the system. An optimized design is desired to avoid any degradation on the output voltage, consume less power, and have less delay in critical path with low supply voltage as we scale toward deep sub-micron technology. Other desired features for the design are to have a small number of transistors to implement the circuit. In particular, for XOR and XNOR circuits, the simultaneous generation of the two-non skewed outputs is highly desirable. As known, the switching speed of the balanced XOR and XNOR functions, comparing with those designs that use an inverter to generate the complement signal, is increased by eliminating the inverter from the critical path. Thus the design methodology for 3-input XOR/XNOR circuits is introduced.

In precise, for XOR and XNOR circuits, the simultaneous generation of the 2-nonskewed outputs is highly desirable [9]. As identified, the switching pace of the balanced XOR and XNOR capabilities, comparing with these designs that use an inverter to generate the complement signal, is expanded through casting off the inverter from the critical path.

II. LITERATURE REVIEW

A new low-voltage high performance CMOS 1-bit full adder circuit is proposed. As of now low-voltage and high performance CMOS one bit full adder circuit is presented. The new design is derived by combining XOR (XNOR) gates used in the traditional full adder [I] and transmission gates established in [Z]. The proposed FA can afford full supply voltage swing at a low supply voltage and offers superior performance in each power and speed than the traditional full adder [I], the transmission full adder [Z], and the low-voltage full adder [9]. The sum and carry generation

circuits of the suggested full adder are intended with hybrid logic patterns. To function at very-low supply voltage, the pass logic circuit that engenders the intermediate XOR and XNOR outputs has been extended to beat the switching delay problem. As full adders are normally employed in a tree structured configuration for prime-efficiency arithmetic circuits, a cascaded simulation constitution is offered to assess the whole adders in a realistic utility environment. A scientific and elegant method to scale the transistor for minimal power-delay product is planned. The circuits being deliberate are augmented for power efficiency at 0.18-mCMOS process technology. With the proposed simulation environment, it's proven that some survival cells in stand-alone operation at low voltage may just fail when cascaded in a bigger circuit, both due to the shortage of drivability or unsatisfactory speed of operation. The proposed hybrid full adder reveals now not best the whole swing good judgment and balanced outputs but additionally robust output drivability. The develop within the transistor depend of its complementary CMOS output stage is compensated through its area efficient layout. For that reason, it remains some of the great contenders for designing massive tree structured arithmetic circuits with reduced power consumption even as keeping the expand in subject to a minimal[10].

By means of the features of full voltage swing at internal nodes and very low short circuit present, HSPICE and Nanosim simulations shown that the proposed full adder presents a power-delay improvement of 36% over the high-quality of different 1-bit full adders that were when compared. A 0.35μm CMOS science and a power deliver of 3.3V have been used to simulate these adders. When used to construct an 8-bits raise-ripple adder, the proposed full adder presents energy savings as much as 28% respect to the other ones[11]. By utilizing hybrid various CMOS and pass transistor logic (PTL) design methods, two novel low-power full swing full adder cores with output driving capability are proposed for top-efficiency embedded structure. The primary design ambitions for these full adder cores are offering no longer only low power and excessive velocity but in addition full-swing operation at a low provide voltage and the riding ability. The simulation outcome exhibit that the proposed full adder core (design-1) is superior to other designs. It consumes 17.69% to 36.21% much less power than three earlier designs excluding 7.87% penalty than CMOS scheme, even as it is 1.88% to 53.64% rapid for sum and 11.64% to 40.67% rapid for carry-out than all reference full adders [12].

The design adopts inverter buffered XOR/XNOR designs to alleviate the threshold voltage loss challenge frequently encountered in pass transistor good judgment design. This problem almost always prevents the whole adder design from working in low supply voltage or cascading instantly without extra buffering. The proposed design successfully embeds the buffering circuit within the full adder design and the transistor count is minimized. The accelerated buffering helps the design function underneath reduce give voltage compared with existing works. It additionally enhances the speed efficiency of the cascaded operation drastically even as preserving the efficiency aspect in power consumption. For performance comparison, each dc and performances of the proposed design towards more than a few full adder designs are evaluated via large HSPICE simulations [13].

The brand new hybrid full adder is composed of pass-transistor good judgment and static CMOS good judgment. The fundamental design ambitions for the whole adder core are delivering no longer most effective low power and excessive speed but additionally with driving potential. Utilizing TSMC CMOS 0.35-μm technology, the characteristics of the experimental circuit when put next with prior literature show that the brand new adder improves 1.8% to 35.6% in power consumption, 11.7% to 41.2% in time delay of Co, and 13.7% to 91.4% in power-extend product of Co. The circuit is validated to have the minimum power consumption and the fastest response of perform signal among the adders selected for evaluation. Because of the low-energy and high-speed, both the brand new OR circuit and the new full adder will also be successfully integrated in a system-on-a-chip (SoC) or an embedded system [14].

III. PROPOSED METHODOLOGY

In this section, design methodology for 3-input XOR/XNOR circuits introduced. This methodology is based on using different basic cells and optimization mechanisms. To obtain basic cells, 3-input XOR/XNOR function is investigated. For choosing the mechanisms, we use the simulation results of [10][11] in which the balanced two inputs XOR/XNOR circuits based on the Cell2 have possessed better results.

A. The Elementary Basic Cell

In the process of designing balanced 3-input XOR–XNOR circuits, we face three independent inputs and two complementary outputs. The elementary basic cell which is extracted of minimum sum of product form of 3-input XOR– XNOR in Eq.1 has been presented in "Fig. 1".

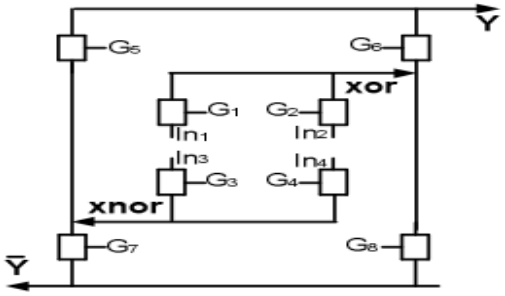


Fig.1 Representation of EBC

This cell has eight elements, deciding two outputs. Each element is a pass transistor or transition gate and has two input controls, i.e., the gate and either the drain or the source.

$$A \oplus B \oplus C = B'.(AC' + A'C) + B.(A'C' + AC)$$

$$A \odot B \odot C = B'.(AC' + A'C) + B'(A'C' + AC)$$

The input indicators (applied to the two input terminals of these transistors) and the determination of pMOS, nMOS transistors and transition gate decide various output states. As provided in "Fig. 1", we consult with the pins of valuable section (IN1 to IN4 and G1 to G4) as A or C, or their enhances respectively. We assume that pins of outside part G5 to G8 will also be B or its complement. One more type of the basic normal telephone is obtained by means of swapping the function of B or its complement that's G5 to G8 and the outputs of principal section which are the drains or the sources of external part. This type of the circuit (as the basic normal telephone) is vigor-less and floor-much less (P-/G-).As a result, the complementary outputs are best littered with input drivability and charged or discharged.

IV. RESULTS AND DISCUSSIONS

By using changing the motives with pass transistors or transmission gates and the control inputs with input signals in combination with optimization and correction mechanisms, a enormous circuit library is applied as each circuit can also be proper for great functions. The decision is pondered to verify dominant mechanisms and cells, in words of power, and lengthen when the optimization goal is PDP. The outcomes are used to provide circuits for prime-performance portable electronic features. Mechanisms contain optimization mechanisms to unravel non-full swing [inverter (I) and feedback (F)], correction mechanisms to get to the backside of high impedance [pull updown network (P) and feedback (F)], or the mixtures of them [bootstrap-pull (BP) up-down, feedback pull (FP) updown, bootstrap-feedback (BF), inverter-feedback (IF), and inverter-pull (IP) up-down]. The cells are divided into two classes:

• Cells with both nMOS and pMOS in EBC structure (C1);

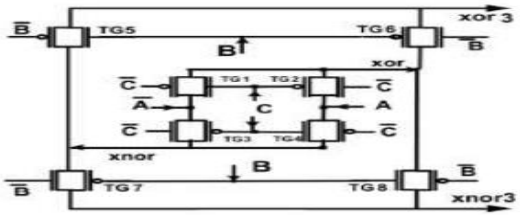
• Handiest nMOS (C2);

To minimize complexity, we've now additionally considered the principal a part of EBC and to gain actual end result, the circuits had been simulated in the chain scan bench.[04] The circuits had been named with the abbreviation of the mechanism (or cell) being utilized, whilst the reverse situations, cells, or mechanisms are assumed to be consistent.

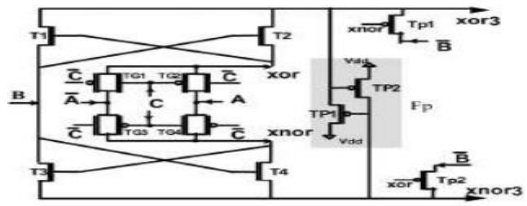
Table 1 Average PDP

Circuits	centeral part				external part				avg
	BC	mechanisms			BC	mechanisms			PDP
		F	B	P		F	B	P	
XO1	TG				C1	Fnp	-	-	1.27
XO2	C2	Fnp	-	-	C2	Fnp	-	-	0.70
XO3	TG				C2	Fp	-	-	0.62
XO4	TG				TG				0.42
XO5	TG				C1	Fnp	-	✓	0.71
XO6	C2	Fnp	-	-	C2	Fnp	-	✓	0.57
XO7	TG				C2	Fp	-	✓	0.47
XO8	TG				C1	-	p&n	✓	0.86
XO9	C2	Fnp	-	-	C2	-	p	✓	0.65
XO10	TG				C2	-	n	✓	0.50

Based on the findings, circuits with names XO1 by way of XO10 are furnished, [08] whose the building constitution small print with the typical PDP are tabulated. Using transmission gates in EBC, which is referred to as TG, the entire circuit is carried out as there is no need for every other mechanisms.[13] accordingly, TG is when put next personally i^{th} others. As a result the brand new 3-input xor/xnor circuits are implemented which is shown within the under fig.4. This need to be drawn on the fundamentals of systematic mobile design methodology utilizing primary long-established mobile phone .The design XO4 and XO7 are the new designs implemented and the power and extend should be analyzed. The corresponding outcome must be denoted in table 2



(a)



(b)

Fig 2 New 3 input Xor/Xnor circuits--(A) XO4 (B) X07

The order of mechanisms in terms of average power and PDP in voltage range from 0.8 to 1.6 V. The PDP detail also demonstrates that there is an inconsistency with the voltage reduction in the mechanism as I has the minimum supply voltage of 0.8V.

Table 2 Performance analysis of delay

Delay (TdnS)	0.8	1.0	1.2	1.4	1.6	Average
X04	0.38ns	1.00ns	1.22ns	1.33ns	1.34ns	1.05ns
X07	1.34ns	1.59ns	1.60ns	1.55ns	1.56ns	1.58ns

Fig.3 shows the output waveforms of XO7, XO4 before the insertion of test bench buffers at 1.2 V. XO7 outputs in some transitions have voltage more than supply voltage that is because of ability of bootstrap in saving voltage. For example, XOR4 output in time 1.05 and XNOR4 output in time 0.38 has voltage 1.33v and 1.35v respectively.

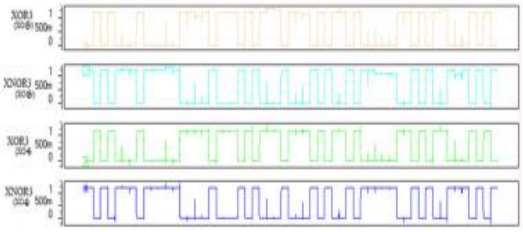


Fig.3. Waveform snapshots of the circuits –XO6 and XO4- in 1.2 V (100 MHz) without test bench output buffers.

V. CONCLUSION

Using cell design methodology and correction optimization mechanisms rely on hybrid-CMOS design style, it is conceived many new 3-input XOR/XNOR circuits. For example, The XO1 to XO6 is presented in the paper that targets low PDP. As a specific function, the important direction of the provided designs includes best two transistors, which explanations low propagation delay. In common, these circuits outperform their counterparts with 17%–53% reduction in energy and 22%-77% reduction in delay respectively, in tanner simulation based on the TSMC 0.125-µm technology.

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