Design of Low Power Vedic Multiplier by Using 180nm Technology

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Abstract- **In the recent years growth of the portable electronic is forcing the designers to optimize the existing design for better performance. Multiplication is the most commonly used arithmetic operation in various applications like DSP processor, math processor and in various scientific arithmetic circuits. Overall performance of the VLSI system is strongly depends on the performance of arithmetic circuits like multiplier. Different types of multiplier are available in the literature depending on the requirement. Designer used different type of multiplier. Power consumption in a multiplier is more prominent design factor in addition with the performance, because portable equipment needs larger battery backup which is only possible through low power design. This work focuses on the reduction of the power dissipations which is showing an ever-increasing growth with the scaling down of the technologies. The power consumption is an important issue that has lead to multiplier designer to adopt different technique to reduce power dissipations. In this work, a Vedic algorithm is used to reduce the power consumption in multiplier used.**

I. INTRODUCTION

In the design of communication circuits, arithmetic circuits, like adders and multipliers, are one of the basic components. The most commonly used components in many digital circuit designs are digital multipliers. To implement any operation, digital multipliers are utilized as they are fast, reliable and efficient components. There are different types of multipliers available, depending upon the arrangement of the components. Based on the application, particular multiplier architecture is chosen. The power dissipation in a multiplier is a very important issue as it reflects the total power dissipated by the circuit and hence affects the performance of the device. Most DSP systems incorporate a multiplication unit to implement algorithms such as correlations, convolution and filtering and frequency analysis. In many DSP algorithms, the multiplier lies in the critical delay path and ultimately determines the performance of the algorithm. Now these days, the speed of multiplication operation is of great importance in DSP as well as in the general processors. In the past, multiplication was implemented generally with a sequence of addition, subtraction and shift operations [19]. Recently, many multiplication algorithms have been invented and developed, each having pros and cons in different fields. To evaluate the efficiency of the processors; a variety of measures can be used. Both the area occupied by the circuit and the time required for the performance of computation must be taken into consideration. The speed of the multiplier is determined by both architecture and circuit. The speed can be expressed by the number of the cell delays along the critical path on the architecture level of the multiplier. The cell delay, which is normally the delay of the adder, is determined by the design of the circuit of the cell. Therefore depending on the speed and area requirements, the digital multipliers used can be either of bit-serial or a bit parallel based architecture. The bit-serial approach processes the data serially where at every clock cycle a single data bit is fed to the processor to be processed. In contrast, the parallel applications processes the data bits in a parallel fashion in just one clock cycle In DSP, digital multipliers are the major source of power dissipation. Due to the switching of a large number of gates during multiplication, there is high power dissipation in these structures. In addition, much power is also dissipated due to a large number of spurious transitions on internal nodes. Timing analysis of a full adder, which is a basic building block in multipliers, has resulted in a different array connection pattern that reduces power dissipation due to the spurious transition activity. Furthermore, this connection pattern also improves the multiplier throughput. In digital electronics, the operation of multiplication is rather simple. It has its origin from the classical algorithm for the product of two binary numbers. This algorithm uses addition and shift left operations to calculate the product of two numbers. Based upon the above procedure, an algorithm can be deduced for any kind of multiplication. At the initial stage, it can also be checked that whether the product will be positive or negative or after getting the whole result, MSB of the results tells the sign of the product.

II. PRESENT WORK (VEDIC MATHEMATICS)

The proposed Vedic multiplier is baesd on the Vedic multiplications formulae (Sutras). This Sutra has been traditionlly used for the Multiplications of two numbers in the decimal number system. In this work

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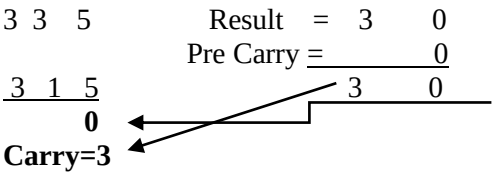
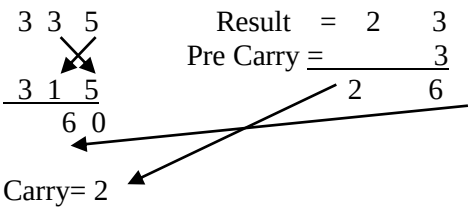
we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. Vedic multiplications based on some algorithm, one of them is discussed below:

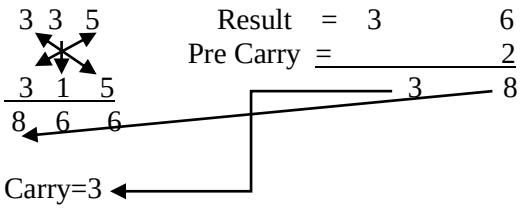
Urdhava Triyakbhyam:-The multiplier is based on an algorithm Urdhava Triyakbhyam (Vertical & Crosswise) of ancient Indian Vedic multiplications. Urdhava Triyakbhyam Sutras is a general multiplications formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel technique through which the generations of all partial products can be done with the concurrent additions of these partial products. The parallelism in generations of partial products and their summations is obtained using Urdhava Triyakbhyam in fig 1. Since the partial products and their sum are calculated in parallel, the multiplier is independent of the clock frequency of the processor. The net advantage is that it reduces the need of microprocessor to operate at increasingly high clock frequency. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipations which results in higher device operating temperature. By adopting the Vedic multiplier, microprocessors designer can easily circumvent these problem to avoid catastrophic device failures.

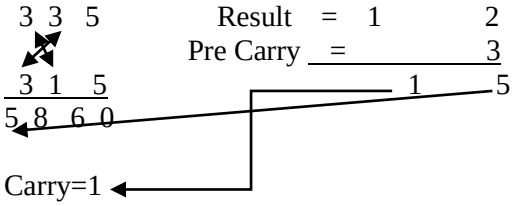
Multiplications of two decimal numbers (335 * 315)

Let us consider the multiplications of two decimal numbers (335 * 315). The digits on the both sides of the lines are multiplied and added with the carry from the previous step. This generates one of the bits of the results and a carry, this carry is added in the next steps and hence processes are going on. If more than one line are added to the previous carry. In each steps least significant bits acts as the results bit and all other bit acts as carry for the next step. Initially the carry is taken to be zero.









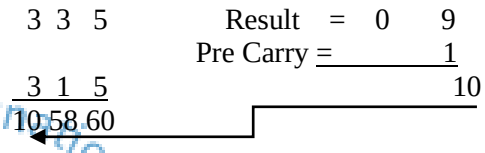


Fig.1:- Multiplications of two decimal numbers by Urdhva Tiryakbhyam

Algorithm for N x N bit Vedic multiplier Using Urdhva Tiryakbhyam for two binary numbers.

For NxN multiplication, divided the multiplicand and multiplier into two parts, consisting of (N to N/2-1) bits and (N/2) bits. For example for multiplications of X and B, of 16 bits each, if X=0000001010101101 then its parts will be 00000010 and 10101101. Represent the above mentioned parts of X as Xm and Xl. Similarly for the B, it is Bm and BL. Now represent X and B as XmXl and BmBl. For A x B we can have

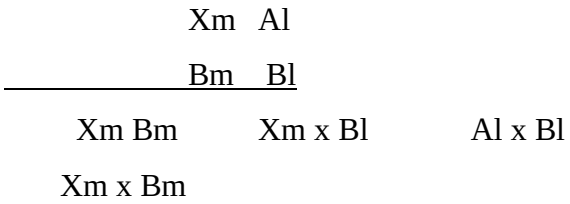


Figure 2:- General Representations of Vedic multiplications

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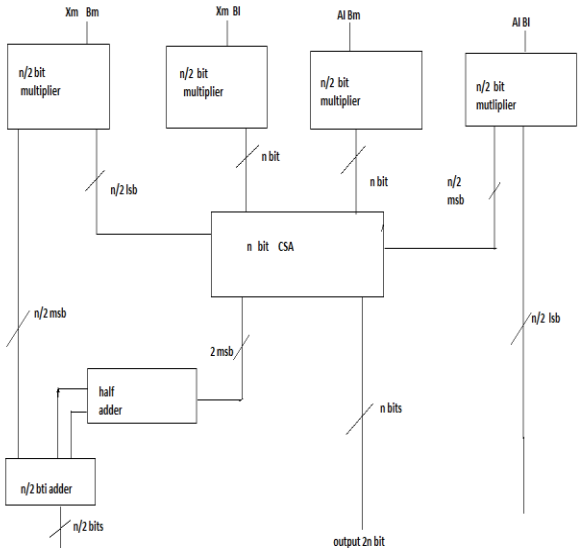

Fig 3:- Complete block diagram for n x n bit Vedic multiplier

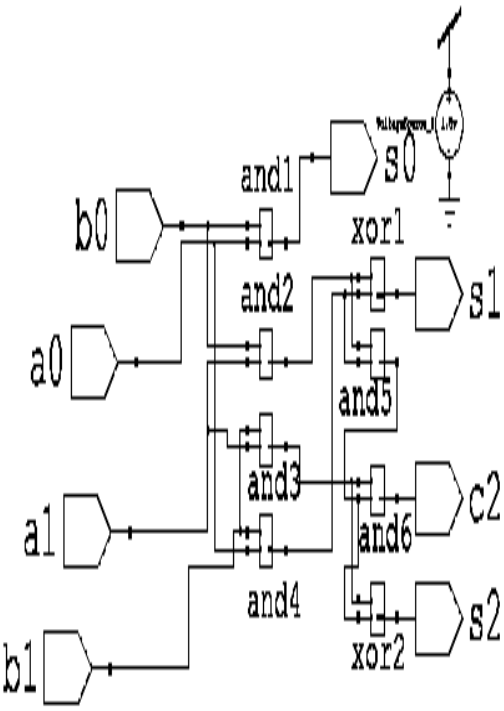

Figure 4: Schematic of 2 bit Vedic Multiplier

Schematic of 2 – bit Vedic Multiplier

The Schematic of 2 – bit Vedic Multiplier design is shown in Figure 4.12. In the 2 bit Multiplier there are basically 2 half adder is used which is combinations of XOR Gate, AND gate is used and four AND Gate is used. In the 2-bit Vedic multiplier a0, b0, a1, b1 are the input of multiplier and s0, s1, c2, s2 are the output of Vedic Multiplier which is shown in fig:-

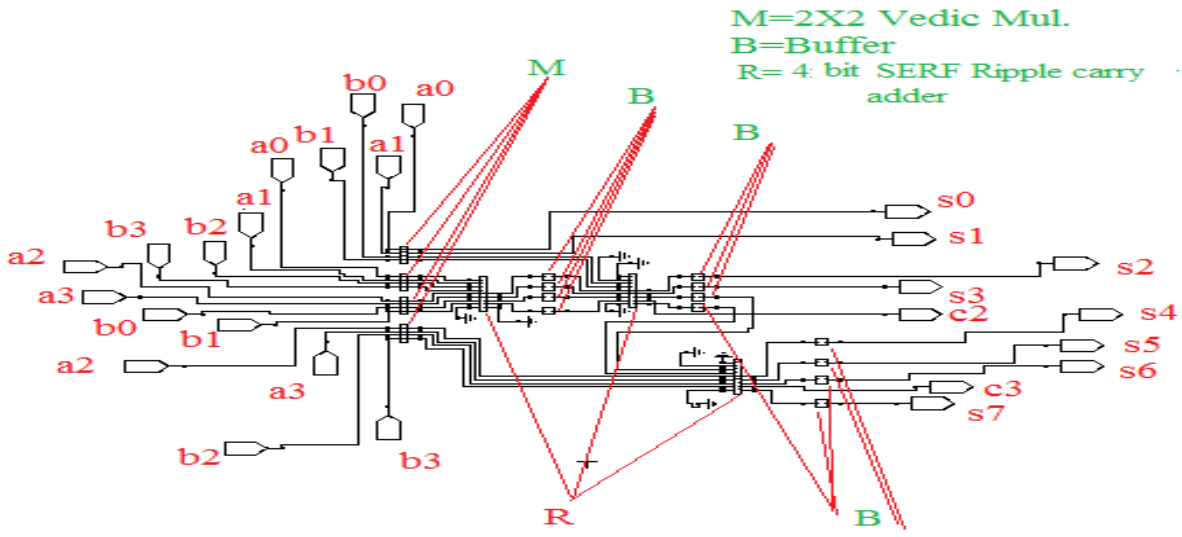

Figure 5: Schematic of 4 – bit Vedic Multiplier using SERF Adder

Simulations Waveform for Vedic Multiplier:- In the 2 bit Vedic multiplier the v (a0) ,v (a1)and v(b0),v (b1) are the input of 2-bit Vedic multiplier and v (s0), v(s1), v(s2), v(c2) is the output of 2-bit Vedic multiplier. Where v (c2) is indicates the carry. The simulations waveform is shown follows:-

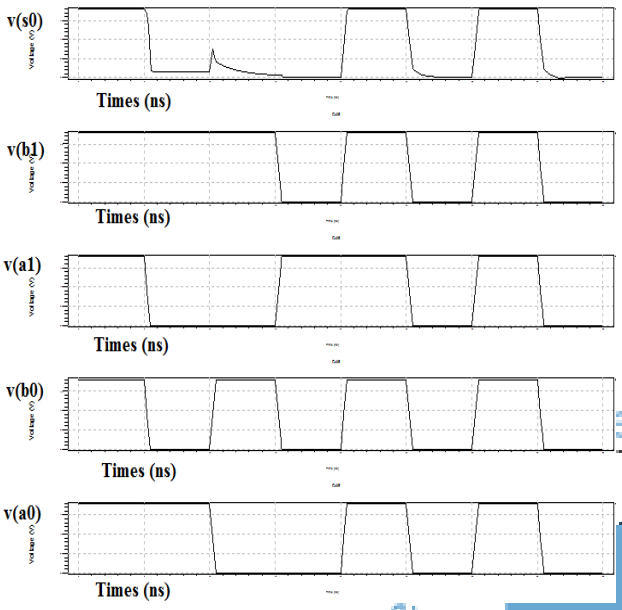

Figure 6: Simulation Waveform of S0

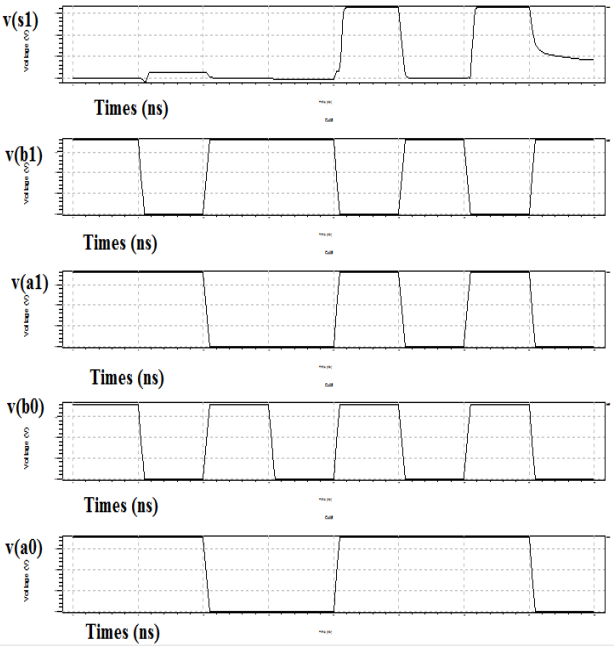

Figure 7: Simulation Waveform of S1

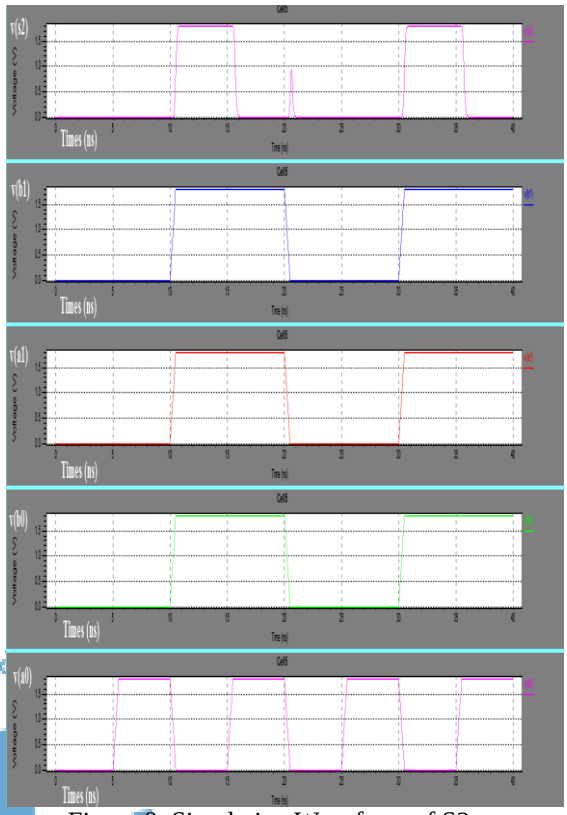

Figure 8: Simulation Waveform of S2

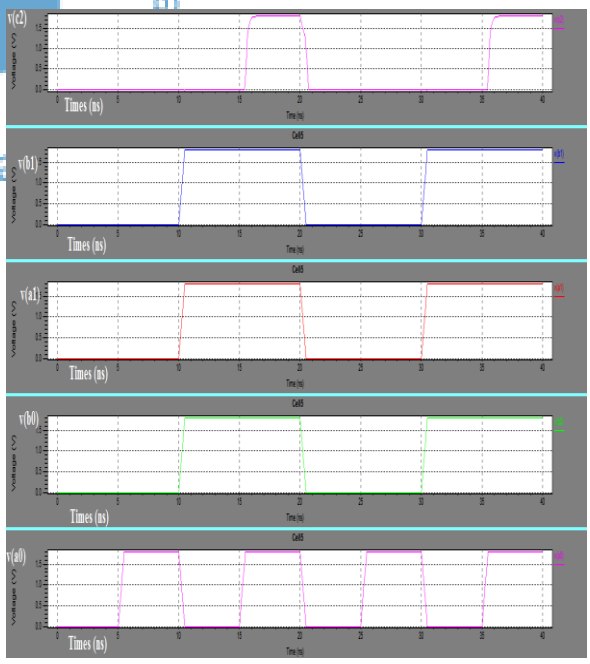

Figure 9: Simulation Waveform of C2

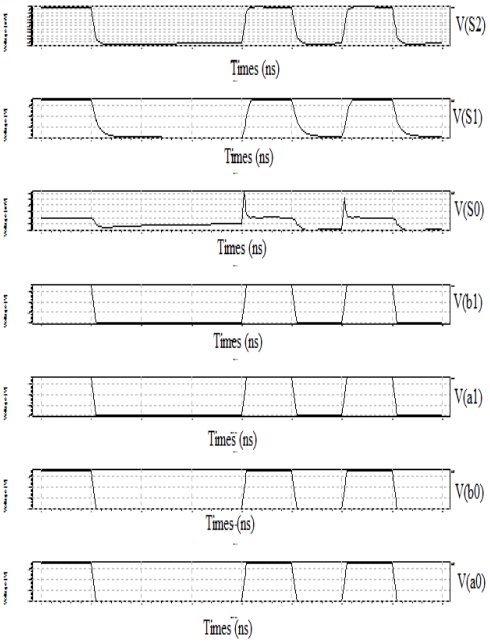

Figure 10: Simulation Waveform of 4 bit Vedic Multiplier Using SERF Adder

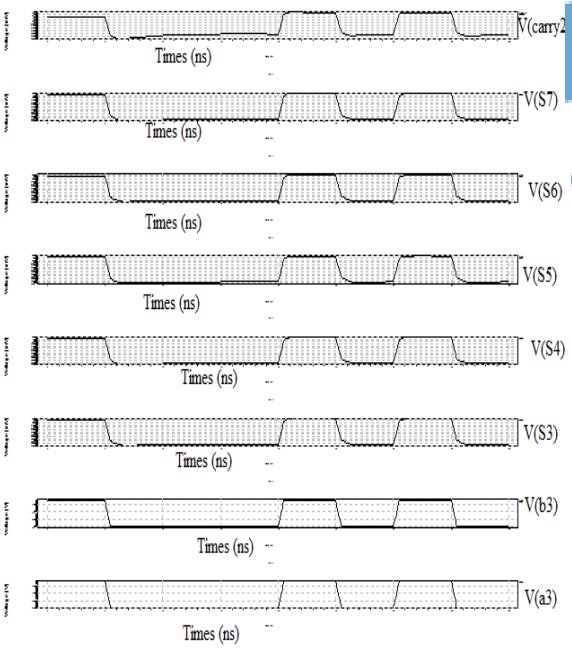

Figure 11: Simulation Waveform of 4 bit Vedic Multiplier Using SERF Adder

III. RESULTS OF VEDIC MULTIPLIERS

Table 1: Transistor of 4-Vedic bit Multipliers

Sr. No.	Multiplier Name	No. of Transistor used
1.	2 X 2 Bit Multiplier	58
2.	4 x 4 bit multiplier using SERF Adder	400
3.	4 x 4 bit multiplier using conventional Adder	520
4.	4 x 4 bit multiplier using 1-bit Full Adder	520
5.	4 x 4 bit multiplier using DPL Adder	616
6.	4 x 4 bit multiplier using Transmissions gate Adder	445

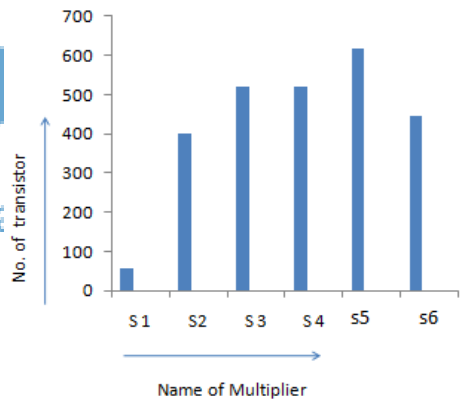

Figure 12:- No. of transistor vs. Name of Multiplier

S1= 2x2 Vedic Multiplier.
S2 = 4 x 4 bit multiplier using SERF Adder. S3=4 x 4 bit multiplier using conventional Adder.
S4=4 x 4 bit multiplier using 1-bit Full Adder. S5=4 x 4 bit multiplier using DPL Adder.
S6=4 x 4 bit multiplier using Transmissions gate Adder.

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Table 2: Power dissipations of 4-Vedic bit Multipliers

Sr. No.	Multiplier Name	Power Dissipations At 500 MHz
1.	2 X 2 Bit Multiplier	0.21µw
2.	4 x 4 bit multiplier using SERF Adder	2.11µw
3.	4 x 4 bit multiplier using conventional Adder	9.55µw
4.	4 x 4 bit multiplier using 1-bit Full Adder	9.07µw
5.	4 x 4 bit multiplier using DPL Adder	4.470µw
6.	4 x 4 bit multiplier using Transmissions gate Adder	0.3.11µw

Table: Propagations Delay of 4-Vedic bit Multiplier

Sr. No.	Multiplier Name	Propagations Delay
1.	2 X 2 Bit Multiplier	0.09ns
2.	4 x 4 bit multiplier using SERF Adder	1.23ns
3.	4 x 4 bit multiplier using conventional Adder	0.39ns
4.	4 x 4 bit multiplier using 1-bit Full Adder	1.45 ns
5.	4 x 4 bit multiplier using DPL Adder	2.31ns
6.	4 x 4 bit multiplier using Transmissions gate Adder	3.01 ns

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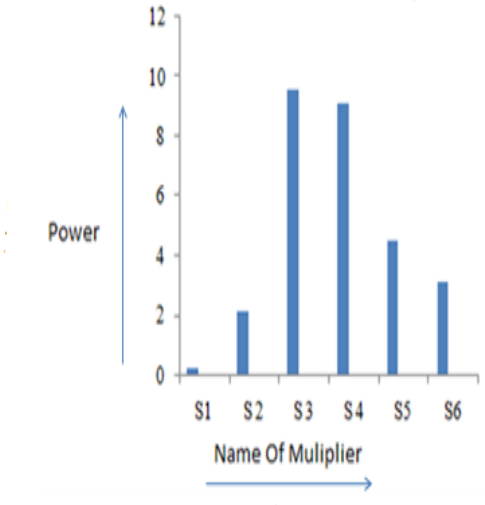


Fig 13:-Average Power vs. Name of Multiplier

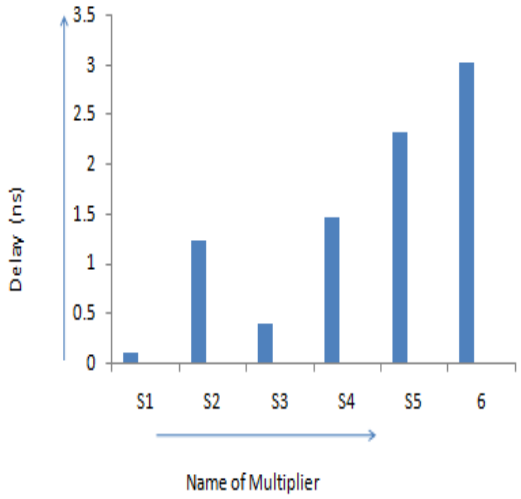


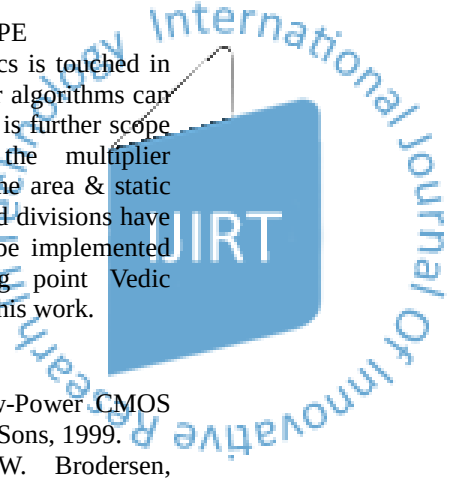
Figure 14:- Delay vs. Name of Multiplier

IV. CONCLUSION

This works focus on optimization of power and high performance of CMOS Vedic multiplier. The comparative analyses of Low power Vedic Multiplier using different adder logic style are done in this thesis. Result shows that the power consumed by the 2 bit Vedic multiplier is 0.21µw and the delay is 0.09ns. The average power consumed by the 4 bit Vedic multiplier using SERF Adder is 2.11µw and the delay 1.23ns. The power consumed by the 4 bit Vedic multiplier by using DPL Adder is 4.470µw and the 4 bit Vedic multiplier using DPL Adder is 2.31ns. The power consumed by the 4 bit Vedic multiplier by using transmission gate is 3.11µw and the delay is 3.01ns. The power consumed by the 4 bit Vedic multiplier using Conventional Adder is 9.55µw and the delay is 0.39ns. The power consumed by the 4 bit Vedic multiplier using 1-bit full Adder is 9.07µw and the delay is 1.45ns. Vedic Multiplier when used by using SERF adder is having lesser power dissipation.

V. FUTURE SCOPE

Only one aspect of Vedic mathematics is touched in this work but there are so many other algorithms can be explored for multiplication. There is further scope of improve implementation of the multiplier presented in this thesis to optimize the area & static power dissipations. Multiplication and divisions have innumerable application which can be implemented using Vedic mathematics. Floating point Vedic processor could be the extensions of this work.



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